Attorney Docket No. LEXA-00301

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

hi ie Application of:

Group Art Unit: 2189

Petro Estakhri et al.

JAN 2 5 2007

Examiner: Denise Tran

Patent No.: 7,155,559 B2 Issued: December 26, 2007 TRANSMITTAL LETTER

Serial No.: 09/648,271

162 North Wolfe Road Sunnyvale, California 94086

Filed: August 25, 2000

(408) 530-9700 Customer No. 28960

For: **FLASH MEMORY** 

ARCHITECTURE WITH SEPARATE STORAGE OF

OVERHEAD AND USER DATA

Attn: Decisions and Certificate of Correction Branch

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Sir:

P

Enclosed is a request for certificate of correction of patent and two copies of form PTO-1050 for filing with the U.S. Patent and Trademark Office.

The Commissioner is authorized to charge any additional fee or credit any overpayment to our Deposit Account No. 08-1275. An originally executed duplicate of this transmittal is enclosed for this purpose.

Respectfully submitted,

HAVERSTOCK & OWENS LLP

THOMAS B. HAVERSTOCK

Reg. No.: 32,571

Attorney for Applicant

CERTIFICATE OF MAILING (37 CFR§ 1.8(a))

Lereby certify that this paper (along with any referred to as using attached or enclosed) is being deposited with the U.S. Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to the: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450

-1-

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Dated: (-23 - 07

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In re Application of:

Petro Estakhri et al.

Patent No.: 7,155,559 B2 Issued: December 26, 2007

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For: FLASH MEMORY

ARCHITECTURE WITH SEPARATE STORAGE OF

OVERHEAD AND USER DATA

Group Art Unit: 2189

Examiner: Denise Tran

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR U.S.P.T.O. MISTAKES UNDER C.F.R. § 1.322

C.F.R. § 1.522

162 North Wolfe Road Sunnyvale, California 94086

(408) 530-9700 Customer No. 28960

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Attn: Decision and Certificate of Correction

**Branch of the Patent Issue Division** 

Sir:

Attached in duplicate is Form PTO-1050, with at least one copy being suitable for printing. The corrections stated in the attached Form PTO-1050 recite the corrections stated below.

Below, column and line numbers refer to U.S. Patent Number 7,155,559 B2, titled "FLASH MEMORY ARCHITECTURE WITH SEPARATE STORAGE OF OVERHEAD AND USER DATA," and issued December 26, 2006. Page and line numbers refer to the corresponding U.S. Patent Application Serial Number 09/648,271, filed August 25, 2000.

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HAVERSTOCK & OWENS LLP.

- 1 -



Attorney Docket No.: LEXA-00301

## CORRECTION OF PATENT OFFICE'S MISTAKES UNDER 37 C.F.R. § 1.322

The following are mistakes made by the U.S. Patent Office. The exact page and line number where the errors are shown correctly in the application file are given below.

#### In the REFERENCES CITED

Under **FOREIGN PATENT DOCUMENTS**, please include "France Patent Number 05-233246". The reference was disclosed to the Examiner in a Supplemental Information Disclosure Statement on September 26, 2003 and again on July 31, 2006 and should have been considered.

Under **FOREIGN PATENT DOCUMENTS**, please include "Japan Patent Number 63-155248". The reference was disclosed to the Examiner in a Supplemental Information Disclosure Statement on October 23, 2003 and considered by the examiner on January 9, 2004 and should have been entered.

#### In the Specification

In Column 5, at Line 58, under **BACKGROUND OF THE INVENTION**, please replace "FRAM cells" with "DRAM cells". The phrase is stated correctly on page 8, Line 16 of the Application filed on August 25, 2000.

In Column 6, at Line 41, under **BACKGROUND OF THE INVENTION**, please replace "LBS's" with "LBA's". The phrase is stated correctly on page 9, Line 16 of the Application filed on August 25, 2000.

In Column 7, at Line 49, under **BACKGROUND OF THE INVENTION**, please replace "VLBA Register 460" with "VLBA Register 360". The phrase is stated correctly on page 10, Line 30 of the Application filed on August 25, 2000.

Respectfully submitted,

HAVERSTOCK & OWENS LLP

Dated: 1-23-67

THOMAS B. HAVERSTOCK

Reg. No.: 32,571

Attorney for Applicant

# UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO. : 7,155,559 B2

DATED: December 26, 2006

INVENTOR(S): Petro Estakhri, Siamack Nemazie

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby correct as shown below:

#### IN THE REFERENCES CITED - FOREIGN PATENT DOCUMENTS

add - - France Patent Number 05-233246 - -.

add - - Japan Patent Number 63-155248 - -.

#### IN THE SPECIFICATION - BACKGROUND OF THE INVENTION

At col. 5, line 58, replace "FRAM cells" with - -DRAM cells - -.

At col. 6, line 41, replace "LBS's" with - - LBA's - -.

At col. 7, line 49, replace "VLBA Register 460" with - - VLBA Register 360 - -.

MAILING ADDRESS OF SENDER: HAVERSTOCK & OWENS LLP 162 North Wolfe Road Sunnyvale, CA 94086 PATENT NO.

No. of add'l copies

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# UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

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